In the Specification

Please amend page 1, line 14 through page 2, line 3 as follows:

A known implementation of the frequency detector is the quadricorrelator concept as in "Digital Logic Implementation of Quadricorrelators for Frequency detectors", by C. G. Yoon, S. Y. Lee and C. W. Lee, IEEE Proc. of 37.sup.th MidWest Symposium on Circuits and Systems, 1994, pp. 757-760. A model for an unbalanced digital quadricorrelator is an unbalanced analog quadricorrelator as shown in FIG. 1. The analog quadricorrelator comprises a first pair of mixers M1, M2 supplied by quadrature signals I, Q and input signal [[INP]] In. Outputs of said pair of mixers M1, M2 are coupled to a pair of low-pass filters L1, L2, the filters providing signals Vi and Vq, respectively. The signal Vi is inputted to a derivation circuit [[D1]] D. The signal Vq and the signal provided by the derivation circuit [[D1]] D are inputted to a third mixer M3, the mixer generating a signal FD, which is indicative for a frequency error between the input signal [[INP]] In and quadrature signals I, Q. In the above-mentioned document a digital implementation of the analog balanced quadricorrelator, is presented. The digital implementation comprises single edge flip-flops coupled to a combinatorial network Hence, the flip-flops detects only phase shifts between quadrature inputs and a rising edge of the D input signal, which means that this quadricorrelator works at half rate or 2* Tbit. Tbit is defined as the time period for a high or a low binary level. Furthermore, the combinatorial part of the quadricorrelator comprises 6 AND gates and 2 OR gates that cause delays or, alternately, phase-shifts between the signals provided by the quadricorrelator.